Express Mail Label No. EV 225206669 US
Date of Deposit: March 26, 2004
Atty. Docket No. 112020.147 US2 (NAN-23)

A FOUR TERMINAL NON-VOLATILE TRANSISTOR DEVICE

Cross-Reference To Related Application

[0001] This application claims the benefit under 35 U.S.C. 119(e) of U.S. Provisional Patent Application No. 60/459,253, filed on March 28, 2003, entitled *Single Transistor with Integrated Nanotube (NT-FET).*

[0002] This application is related to the following U.S. applications, the contents of which are incorporated herein in their entirety by reference:

> U.S. Provisional Apl. Ser. No. 60/459,223 filed on March 28, 2003, entitled *NRAM Bit Selectable Two-Device Nanotube Array*; and U.S. Pat. Apl., Ser. No. (inserted upon USPTO designation), filed on the same day as the present application, entitled *NRAM Bit Selectable Two-Device Nanotube Array.*
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> U.S. Provisional Apl. Ser. No. 60/459,222 filed on March 28, 2003, entitled *NRAM Byte/Block Released Bit Selectable One-Device Nanotube Array*; and U.S. Pat. Apl., Ser. No. (inserted upon USPTO designation), filed on the same day as the present application, entitled *Non-Volatile Ram Cell and Array Using Nanotube Switch Position for Information State.*
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> U.S. Provisional Patent Application No. 60/459,224, filed on March 28, 2003, entitled *Nanotube-on-Gate FET Structures and Applications*; and U.S. Pat. Apl, Ser. No. (inserted upon USPTO designation), filed on the same day as the present application, entitled *Nanotube-on-Gate FET Structures and Applications.*

Background

1. Technical Field

[0003] The invention relates to non-volatile transistors and particularly to non-volatile transistors using nanotube (NT) switching components.

2. Discussion of Related Art

[0004] Important characteristics for a memory cell in electronic device are low cost, nonvolatility, high density, low power, and high speed. Conventional memory solutions include Read Only Memory (ROM), Programmable Read only Memory (PROM), Electrically Programmable Memory (EPROM), Electrically Erasable Programmable

Read Only Memory (EEPROM), Dynamic Random Access Memory (DRAM), and Static Random Access Memory (SRAM).

[0005] ROM is relatively low cost but cannot be rewritten. PROM can be electrically programmed but with only a single write cycle. EPROM has read cycles that are fast relative to ROM and PROM read cycles, but has relatively long erase times and reliability only over a few iterative read/write cycles. EEPROM (or "Flash") is inexpensive, and has low power consumption but has long write cycles (ms) and low relative speed in comparison to DRAM or SRAM. Flash also has a finite number of read/write cycles leading to low long-term reliability. ROM, PROM, EPROM, and EEPROM are all non-volatile, meaning that if power to the memory is interrupted the memory will retain the information stored in the memory cells.

[0006] DRAM stores charge on transistor gates that act as capacitors but must be electrically refreshed every few milliseconds complicating system design by requiring separate circuitry to "refresh" the memory contents before the capacitors discharge. SRAM does not need to be refreshed and is fast relative to DRAM, but has lower density and is more expensive relative to DRAM. Both SRAM and DRAM are volatile, meaning that if power to the memory is interrupted the memory will lose the information stored in the memory cells.

[0007] Consequently, existing technologies are either non-volatile but are not randomly accessible and have low density, high cost, and limited ability to allow multiples writes with high reliability of the circuit's function, or they are volatile and complicate system design or have low density. Some emerging technologies have attempted to address these shortcomings.

[0008] For example, magnetic RAM (MRAM) or ferromagnetic RAM (FRAM) utilizes the orientation of magnetization or a ferromagnetic region to generate a nonvolatile memory cell. MRAM utilizes a magnetoresistive memory element involving the anisotropic magnetoresistance or giant magnetoresistance of ferromagnetic materials yielding nonvolatility. Both of these types of memory cells have relatively high resistance and low-density. A different memory cell based upon magnetic tunnel junctions has also been examined but has not led to large-scale commercialized MRAM

devices. FRAM uses a circuit architecture similar to DRAM but which uses a thin film ferroelectric capacitor. This capacitor is purported to retain its electrical polarization after an externally applied electric field is removed yielding a nonvolatile memory. FRAM suffers from a large memory cell size, and it is difficult to manufacture as a large-scale integrated component. See U.S. Patent Nos. 4853893, 4888630, and 5198994.

[0009] Another technology having non-volatile memory is phase change memory. This technology stores information via a structural phase change in thin-film alloys incorporating elements such as selenium or tellurium. These alloys are purported to remain stable in both crystalline and amorphous states allowing the formation of a bi-stable switch. While the nonvolatility condition is met, this technology appears to suffer from slow operations, difficulty of manufacture and reliability and has not reached a state of commercialization. See U.S. Patent Nos. 3448302, 4845533, 4876667, and 6044008.

[0010] Wire crossbar memory (MWCM) has also been proposed. See U.S. Patent Nos. 6128214, 6159620, and 6198655. These memory proposals envision molecules as bi-stable switches. Two wires (either a metal or semiconducting type) have a layer of molecules or molecule compounds sandwiched in between. Chemical assembly and electrochemical oxidation or reduction are used to generate an "on" or "off" state. This form of memory requires highly specialized wire junctions and may not retain non-volatility owing to the inherent instability found in redox processes.

[0011] Recently, memory devices have been proposed which use nanoscopic wires, such as single-walled carbon nanotubes, to form crossbar junctions to serve as memory cells. See WO 01/03208, Nanoscopic Wire-Based Devices, Arrays, and Methods of Their Manufacture; and Thomas Rueckes et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing," Science, vol. 289, pp. 94-97, 7 July, 2000. Hereinafter these devices are called nanotube wire crossbar memories (NTWCMs). Under these proposals, individual single-walled nanotube wires suspended over other wires define memory cells. Electrical signals are written to one or both wires to cause them to physically attract or repel relative to one another. Each physical state (i.e., attracted or repelled wires) corresponds to an electrical state. Repelled wires are an open circuit junction. Attracted wires are a closed state forming a rectified junction.

When electrical power is removed from the junction, the wires retain their physical (and thus electrical) state thereby forming a non-volatile memory cell.

[0012] The NTWCM proposals to date rely on directed growth or chemical self-assembly techniques to grow the individual nanotubes needed for the memory cells. These techniques are now believed to be difficult to employ at commercial scales using modern technology. Moreover, they may contain inherent limitations such as the length of the nanotubes that may be grown reliably using these techniques, and it may difficult to control the statistical variance of geometries of nanotube wires so grown.

[0013] The ideal memory for at least some purposes is one which would offer low cost per bit, high density, fast random access, read/write cycle times of equal duration, low power consumption, operation over a wide temperature range, a single low-voltage power supply, with a high degree of radiation tolerance. The non-volatile described herein cell offers high speed read, but also high speed write (nanosecond) versus the slow (microsecond & millisecond) write time of EEPROM and FLASH EEPROM type of memories. The memory is much denser than conventional SRAM because it has a two-device, NT and 3-array line structure, and offers competitive performance. The density is less than that of DRAM cells, however, the product offers NDRO operation and non-volatility.

[0014] U.S. Patent Publication No. 2003-0021966 discloses, among other things, electromechanical circuits, such as memory cells, in which circuits include a structure having electrically conductive traces and supports extending from a surface of a substrate. Nanotube ribbons that can electromechanically deform, or switch are suspended by the supports that cross the electrically conductive traces. Each ribbon comprises one or more nanotubes. The ribbons are typically formed from selectively removing material from a layer or matted fabric of nanotubes.

[0015] For example, as disclosed in U.S. Patent Publication No. 2003-0021966, a nanofabric may be patterned into ribbons, and the ribbons can be used as a component to create non-volatile electromechanical memory cells. The ribbon is electromechanically-deflectable in response to electrical stimulus of control traces and/or the ribbon. The deflected, physical state of the ribbon may be made to represent a corresponding

information state. The deflected, physical state has non-volatile properties, meaning the ribbon retains its physical (and therefore informational) state even if power to the memory cell is removed. As explained in U.S. Patent Publication No. 2003-0124325, three-trace architectures may be used for electromechanical memory cells, in which the two of the traces are electrodes to control the deflection of the ribbon.

Summary

[0016] The invention provides non-volatile transistor devices. According to one aspect of the invention, a non-volatile transistor device includes a source region and a drain region of a first semiconductor type of material and each in electrical communication with a respective terminal. A channel region of a second semiconductor type of material is disposed between the source and drain region. A gate structure is made of at least one of semiconductive or conductive material and disposed on an insulator over the channel region and is not in permanent contact with a corresponding terminal. A control gate is made of at least one of semiconductive or conductive material and in electrical communication with a respective terminal. An electromechanically-deflectable nanotube switching element is in electrical communication with one of the gate structure and the control gate structure and is positioned to be electromechanically deflectable into contact with the other of the gate structure and the control gate structure. When the nanotube switching element is in communication with both the control gate and the gate structure, the control gate may be used to modulate the conductivity of the channel region.

[0017] According to another aspect of the invention, the transistor gate is embedded in and surrounded by an insulator material. The channel region resistance is modulated by the transistor gate voltage capacitively coupled to the channel region. When the electromechanically deflectable nanotube switching element switches into contact with the control gate element, electric charges briefly flow to charge the internal gate capacitance network, including the capacitor between transistor gate and channel regions. No electrical current flows because the transistor gate is surrounded by insulating material. The absence of electrical current flow as the nanotube switching element comes

into contact with the control gate may be referred to as cold switching, and maximizes the allowed number of contact/release cycles. Typically, the expected number of allowable contact/release cycles is in excess of 10^{15} cycles.

[0018] According to another aspect of the invention, the nanotube switching element is an article formed from a porous fabric of nanotubes.

[0019] According to another aspect of the invention, the fabric is substantially a monolayer of nanotubes.

[0020] According to another aspect of the invention, the nanotubes are single-walled carbon nanotubes.

[0021] According to another aspect of the invention, the source and drain regions are disposed on or in a horizontal substrate and wherein the nanotube article is suspended vertically in relation to the horizontal substrate.

[0022] According to another aspect of the invention, the nanotube article is in physical and electrical contact with the gate structure.

[0023] According to another aspect of the invention, the device further includes a release gate and release node positioned in spaced relation to the nanotube switching element, wherein, in response to a signal on the release node, the release gate electromechanically deflects the nanotube switching element out of contact with the one of the control gate and the gate structure.

[0024] According to another aspect of the invention, the release gate surface is coated with an insulating, semiconducting, or conducting layer.

[0025] According to another aspect of the invention, the contact between the nanotube switching element and the one of the control gate and gate structureis a non-volatile state.

[0026] According to another aspect of the invention, the contact between the nanotube switching element and the insulating, semiconducting, or conducting layer on the release gate is a non-volatile state.

[0027] According to another aspect of the invention, the device occupies an area of $8F^2$.

[0028] According to another aspect of the invention, an array of such devices is

provided in which a release node is shared among at least two adjacent devices.

Brief Description of the Drawing

[0029] In the Drawing,

Figures 1a and 1b are circuit schematics, illustrating two states of a four terminal non-volatile transistor device of certain embodiments of the invention;

Figures 2a and 2b are circuit schematics, illustrating two physical arrangements of a four terminal non-volatile transistor device of certain embodiments of the invention;

Figures 3a and 3b are circuit schematics, illustrating one state of a four terminal non-volatile transistor device of certain embodiments of the invention and illustrating inherent capacitances of such a device in such a state;

Figure 4a depicts the channel region below one terminal of the four terminal device, when modulated in a particular way;

Figure 4b depicts the channel region below one terminal of the four terminal device when modulated in a different way than that of Figure 4a;

Figure 5a depicts the switching or writing of the four terminal device and the corresponding conditions to effect such;

Figure 5b depicts the switching or writing of the four terminal device and the corresponding conditions to effect such;

Figure 6 is a plan view of a physical layout of a four terminal device according to certain embodiments of the invention;

Figure 7 is a cross sectional view along axis AA' of Figure 6.The release plate includes an insulating, semiconducting, or conducting layer;

Figure 8 is a cross sectional view along axis BB' of Figure 6;

Figure 9 is a schematic for an 8-bit array NRAM array based on the cell layout of Figure 6;

Figure 10 illustrates the operating voltages of the array of Figure 9 in a block release mode; and

Figure11 illustrates voltages of the array of Figure 9 in single bit or nibble release modes.

Detailed Description

[0030] Preferred embodiments of the invention provide a four terminal non-volatile transistor device. These embodiments, in essence, integrate a nanotube (NT) structure (such as a nanofabric article or ribbon) with a FET transistor. In preferred cases, the NT is integrated in such a way that external transistor connections are made only to the FET transistor terminals for deflecting the NT element into contact with the control gate, and the NT is switched internal to the device. The release gate is accessed directly. However, there is no direct contact to the NT element itself. Such a device is referred to as an NT-FET (nanotube-FET) device herein, and its construction and operation are described below.

[0031] The single transistor NT-FET can be used in many applications, for example, an NRAM memory array of very small cell size. When used in such a non-volatile memory array, preferred layout designs occupy less than 8 F^2 cell area with bit selectivity for read, release, and write operations. There are many other applications because the NT-FET transistor is such a versatile active electrical element. For example, NT-FET devices in product chips can be used to repeatedly change on-chip generated timings and voltages after fabrication at the wafer level, or after chip assembly at the module, card, or system level. This can be done at the factory, or remotely in field locations. Such usage can enhance product yield, lower power, improve performance, and enhance reliability in a wide variety of products.

[0032] A preferred NT-FET device has four terminals as shown in Figures 1a-b: a control gate (CG), source (S), drain (D), and a reset gate (RG). A floating gate (FG) and nanotube (NT) structure are combined to form a single floating gate nanotube (FGNT) element. The FGNT interacts with control gate (CG), release gate (RG) and the FET channel as described below.

[0033] Figure 1a illustrates the NT-FET in an OFF state in which the FGNT is electrically isolated from the terminals. This state is non-volatile. Figure 1b illustrates the NT-FET in an ON state in which the FGNT is electrically connected to control gate CG. This state is also non-volatile.

[0034] Preferred embodiments include NFET and PFET CMOS devices, particularly NFET array devices in combination with nanotube electromechanical (NT) switch elements to provide unit cells that may be employed in integrated circuits. The nanotube electromechanical switch elements are formed from matted, porous fabrics of nanotubes as described below.

[0035] The NT is attached mechanically and electrically to a polysilicon floating gate to form the FGNT element that, in combination with CG, controls the channel of the NT-FET between the source (S) and drain (D) terminals. Switching the FGNT from the OFF state to the ON state, as shown in Figure 1, is controlled by applying appropriate voltages $V_{NT\ SELECT}$ between CG and FGNT. Switching from the ON state to the OFF state is controlled by the difference in voltage $V_{NT\ RELEASE}$ between the release gate RG and floating gate nanotube element FGNT. Typical read and write operating voltages for the NT-FET device is in the range of 1 to 2.5 volts. Release operations require a higher voltage.

[0036] The NT carbon fabric is suspended between control gate CG and release gate RG. As shown in Figure 2a-b, the suspended NT fabric may be suspended horizontally or vertically. Typical suspended NT lengths are in the 90 – 180 nm range with gaps in the 5 – 30 nm range, for example.

[0037] The NT-FET device operation requires modulation of the channel region between the drain D and source S to make the channel conductive or not. This modulation is affected by a combination of voltages applied to control gate CG, drain D, and capacitive coupling effects. The capacitive coupling is between control gate CG, floating gate nanotube element FGNT, and the channel region (analogous to that in EPROM, EEPROM, and Flash EEPROM device structures).

[0038] Figure 3 illustrates key capacitance coupling in the NT-FET device structure. The capacitance values C_{12}, C_{23}, C_{27} and C_{36} are a function of material properties, film thicknesses, and the layout area (design) of the capacitor plates. Capacitance C_{12} is the capacitance between like numeral identified elements; e.g., control gate 1 and floating gate nanotube element 2. In addition, capacitance C_{36} is a voltage-dependent capacitance modulated by drain voltage Vd. Figure 3 illustrates key capacitance coupling between

elements of the NT-FET device structure. Figure 3a illustrates a device schematic with elements numbered to correspond to coupling capacitances. Figure 3b illustrates a simplified cross section of the physical location of key coupling capacitors.

[0039] When the NT-FET device is in the OFF state, the coupling ratios of these capacitances determine the voltage V_{FGNT}, as is further explained in connection with Figure 4. Capacitance C_{27} is much smaller than capacitors C_{12} and C_{23} (by design), and its effect is ignored for these calculations.

[0040] Figure 4 focuses on the channel region below gate FGNT. Sufficient voltage to the control gate V_{CG} has been applied such that the voltage on the floating gate nanotube element V_{FGNT} exceeds the threshold voltage V_{TH} to invert the channel region to make it conductive between drain and source. The source voltage Vs in this case floats (not forced). If the drain voltage Vd equals 0, then the inverted channel is at zero voltage, and voltage dependent capacitance C_{36} is not part of the capacitance ratio controlling V_{FGNT} as illustrated in Figure 4a. In addition, FGNT is relatively tightly coupled to the inverted channel. If, on the other hand, the drain voltage is positive, electrons flow from the channel region and the channel is depleted. FGNT to channel capacitance C_{23} is now in series with voltage modulated depletion capacitor C_{36} as illustrated in Figure 4b. Since C_{36} is typically 1/5 the value of C_{23} for this type of structure, FGNT is decoupled from the FET channel region.

[0041] Figure 5 illustrates the operations for switching of the NT-FET transistor to write a 0 or 1. The select voltage is applied between the control gate CG and floating gate nanotube element FGNT. The voltage levels internal to the NT-FET device are a function of the external applied voltages and the capacitor ratios internal to the NT-FET device. The representative voltages were calculated using relative capacitance values. In this case, C_{12} equals C_{23}, and the value for C_{36} is 1/5 of C_{23}.

[0042] Write "1" refers to the transition of NT-FET from the OFF to the ON state. Figure 5a illustrates the conditions for maximizing select voltage $V_{NT\ SELECT}$ for NT switching (ohmic-like contact with CG). Figure 5b illustrates the conditions to minimize the $V_{NT\ SELECT}$ voltage so that NT is unchanged and remains in the OFF state. In

operation, an NT structure with a select voltage threshold above 0.4 volts but less than 1.25 volts may be used for a switching (write) operation.

[0043] Detecting or reading the ON or OFF state of the device is as follows. If the NT-FET device is in the ON state, CG is electrically connected to the floating gate nanotube element FGNT. For an FET device threshold of 0.7 volts, for example, V_{CG} equals V_{FGNT} which equals 1 volt. This forms a conductive channel between source and drain. If, however, the NT-FET device is in the OFF state, then for a control voltage V_{CG} equals 1 volt and C_{12} equals C_{23}, the FET gate voltage V_{FGNT} equals 0.5 volts and no channel is formed between source and drain. Note that when reading a device in the OFF state, $V_{CG} - V_{FGNT} = 0.5$ volts, so that the select threshold voltage range needs to be above 0.5 volts but less than 1.25 volts to prevent an unwanted OFF to ON write transition during the read operation.

[0044] Release operations use a voltage applied between release gate RG and floating gate nanotube element FGNT. Release voltages will range in the 2.1 to 6.5 volt range, depending on block versus bit level release considerations, as described below.

[0045] Figure 5 illustrates the write mechanism based on applied voltages and relative capacitance values. The NT select voltage range shown was calculated for the write operation. Figure 5a illustrates conditions to switch the NT-FET device from the OFF to ON (write "1") state. Figure 5b illustrates conditions to maintain the NT-FET device in the OFF state.

[0046] The NT-FET device may be used for very dense NRAM memory array as illustrated in top view in Figure 6. A cell boundary is shown and labeled CELL. The word line WL forms the control gate CG. The release line RL contacts RG. There typically is a covering layer and a release gap between RG and NT, such a covering layer may be made from insulating, semiconducting, or metallic material. Array symmetry allows RG gate sharing between two adjacent cells. Array lines RL and RG are orthogonal to enable a single bit release option. The NTs are mounted in the vertical direction. The source diffusion is continuous between cells. Drain diffusions are shared between two adjacent cells and are contacted by a bit line BL. The BLs and WLs are ideally orthogonal.

[0047] Cross section AA' is cut through the a bit line BL, bit line diffusion contact, the device along the FET channel, the NT devices, word line WL, and release gate RG. Figure 7 is a cross-sectional view of a cell taken along line AA'. In this arrangement, the nanotube elements NT are suspended vertically, as suggested in Figure 2b, and illustrated in a vertical and un-deflected position. In the ON state (store a "1"), nanotube element NT is in contact with CG. In the OFF state (store a "0"), nanotube element NT is in contact with RG the insulating, semiconducting, or metallic material covering layer.

[0048] Cross section BB' of Figure 6 is cut through and along release line RL, RG and RL-RG contact, WL and FGNT over the field region of the FET device, and shared source S diffusion. Figure 8 is a cross-sectional view of a cell taken along line BB'.

[0049] Figure 9 is a schematic for an 8-bit array NRAM array based on the cell layout of Figure 6. The array is composed of eight non-volatile memory (storage) cells labeled 0 to 7 using the integrated NT-FET device. The memory array includes word, bit, and release lines that are selected by decoders (not shown), and sense amplifiers (not shown) to detect the state (ON or OFF) of the array cells. The array of Figure 9 may be a sub-array of a much larger memory. Typical operating voltages are applied to the array using word lines, bit lines, and release lines. The resulting internal cell voltages are calculated as described in connection with the descriptions of Figures 3, 4, and 5. These calculations give typical FET device operating voltages for gate, source, and drain. Corresponding NT operating ranges for select and release modes are calculated. The array of Figure 9 may be operated in several release modes. The chosen mode of operation determines the required NT select and release voltage operating ranges.

[0050] Three release operating modes were considered: block, nibble (1/2 byte), and single bit release. For the array in Figure 9, the block mode results in the simultaneous release of all NT-FETs in all eight array cells. For the nibble release mode, four of the eight NT-FETs in the eight array cells are simultaneously released. For single bit release, only one NT-FET is released out of the eight cells in the array. The block release mode is the simplest and results in the broadest range of NT release voltages. The other release modes are more restrictive because some of the array cells of Figure 9 are not released, and this requirement introduces additional electrical constraints.

[0051] Figure 10 shows the operating voltages of the array of Figure 9 applied to Cell 0. Cell 0 operation is the same as that of all array cells (cells 0-7). In Figure 10, a block release mode is employed such that cells 0-7 are all simultaneously released. Prior to release, individual cells may be in the ON or OFF state. During the release time interval, if Cell 0 is in the ON state, then Cell 0 switches to the OFF state. If, however, Cell 0 is in the OFF state, then Cell 0 remains in the OFF state. The externally applied voltages to the terminals of device NT-FET0 in array Cell 0 are WL0 driving CG0, RL0 driving RG0, BL0 driving drain diffusion D0, and the voltage applied to the shared source S0 (not shown). These externally applied voltages couple to the internal nodes of device NT-FET0, as explained in connection with the description of Figures 3, 4, 5, and result in the internal voltage applied to FGNT0. The combination of external and internal voltages results in the $V_{NT\ RELEASE}$ and $V_{NT\ SELECT}$ used to activate nanotube NT0 during release and write operations.

[0052] In the example illustrated in Figure 10, a release voltage of 6.5 volts was chosen. However, 10 volts may be applied, for example, without affecting the array devices. The maximum voltage that can be applied is limited by the RL0 peripheral driver considerations because RG0 to FGNT0 capacitance C_{27} is small. If the array device prior to release is in the ON state, then word line WL0 is electrically connected to FGNT0, and FGNT0 is held at ground by WL0. If the array device prior to release is in the OFF state, then FGNT0 is not directly coupled to WL0, but remains near ground because of capacitive coupling to WL0, and negligible capacitive coupling between FGNT0 and RN0 (RN0 is connected to RL0). Therefore, if RL0 is driven up to 6.5 volts, then $V_{NT\ RELEASE} = 6.5$ volts is applied through the insulator layer and across the release gap of NT0, ensuring that NT0 is in the OFF state prior to write as illustrated in Figure 10. The release voltage may be sufficiently high to cause NT to deflect into contact with, or into close proximity to, the insulating layer on RG, with NT held in the "OFF" state by van der Waals forces. The release threshold of NT0 for this example is $V_{NT\ REL\ TH} < 6.5$ volts. During write, $V_{NT\ RELEASE}$ can reach -2.1 volts. To ensure that release cannot occur during write, the release threshold voltage requirement is $|2.1| < V_{NT\ REL\ TH} < 6.5$ volts.

[0053] The write operation is preceded by a release operation so that device NT-FET0 of Cell 0 is in the OFF state. To turn device NT-FET0 ON, the bit line BL0 voltage Vd equals 0. The FGNT0 voltage transition is controlled by capacitance coupling and reaches 1.25 volts as WL0 voltage transitions to 2.5 volts as illustrated in Figure 5. Therefore, the NT0 select voltage $V_{NT\,SELECT}$ equals 1.25 volts as shown in Figure 10. For a NT0 structure with select threshold $V_{NT\,SEL\,TH}$ less than 1.25 volts, device NT-FET0 switches to the ON state. To leave device NT-FET0 in the OFF state, Vd is held in the 1 to 2.5 volt range. FGNT0 transitions to 2.1 volts as illustrated in Figure 5. Therefore, the NT0 select voltage is limited to $V_{NT\,SELECT}$ equals 0.4 volts. For a NT0 structure with select threshold $V_{NT\,SEL\,TH}$ greater than 0.4 volts, device NT-FET0 remains in the OFF condition. The NT0 structure threshold voltage requirement during write mode is $V_{NT\,SEL\,TH}$ greater than 0.4 volts and less than 1.25 volts. The source voltage Vs (not shown) is left in open (not used) during the write operation.

[0054] During the read operation, BL0 is selected by the peripheral bit decoder/driver (not shown), set high and released at Vd equal to 1 volt. The common source is held at Vs equal to 0 volts. WL0 transitions to 1 volt. If NT-FET0 is in the ON state, then FGNT0 transitions to 1 volt since FGNT0 is electrically connected. If the FET threshold voltage V_{TH} of device NT-FET0 is 0.7 volts, then the channel region is inverted and bit line BL0 is discharged. If, however, NT-FET0 is in the OFF state, then word line WL0 voltage is capacitively coupled to FGNT0, with FGNT0 switching to 0.5 volts. For an FET threshold voltage V_{TH} equal to 0.7 volts, the FET channel of device NT-FET0 remains off, and the BL0 is not discharged.

[0055] For the single bit release mode, the read and write waveforms of Figure 10 are unchanged. However, the release waveforms are changed as shown in Figure 11. If Cell 0 is to be released, then RL0 is switched to 6.5 V with WL0 at 0 volts as previously discussed. However, if another cell such as Cell 1 NT-FET1 is to be released, without disturbing the state of NT-FET0 in Cell 0, then the WL0 voltage must be increased to reduce the release voltage $V_{NT\,RELEASE}$ to a value below the release threshold voltage $V_{NT\,REL\,TH}$. This in turn increases the voltage on gate FGNT0. The source and drain voltages of device NT-FET0 are held at the same voltage so no current flows in the FET

channel during the release mode. The voltage applied to WL0 (CG0) is limited by the voltage across the gate oxide of NT-FET0, especially in the ON state, when FGNT0 and CG0 are electrically connected. Assuming a gate oxide voltage limit of 3.5 volts, then the WL0 voltage limit is 3.5 volts. To prevent the RL0 voltage of 6.5 volts from releasing NT0 of device NT-FET0, WL0 is switched to 3.5 volts. The release voltage $V_{NT\,RELEASE}$ in Cell 0 is reduced to 3.0 volts. If the release threshold $V_{NT\,REL\,TH}$ voltage of NT0 is greater than 3.0 volts, NT-FET0 remains unchanged. Then, $V_{NT\,REL\,TH}$ is greater than 3 volts and less than 6.5 volts becomes the release voltage range for the single bit release mode of operation. Nibble (4 bit, ½ byte release) allows half the array to be released simultaneously. Since not all bits are released simultaneously, the same release voltage range of $V_{NT\,REL\,TH}$ greater than 3.0 volts and less than 6.5 volts is used as in the single bit release mode.

[0056] Under preferred embodiments, a NT element and an FET device are effectively integrated into a single non-volatile device referred to as a NT-FET device. The external read and write voltages are low, in the 1 to 2.5 volt range, and the device operates at low voltage and current values. The release voltage is at least 6.5 volts, but has minimal effect on the internal NT-FET capacitance coupled voltages, because the release gate RG to FGNT capacitance C_{27} is very small as a consequence of the array structure/layout. Layout of an NRAM cell based on the NT-FET device can produce a cell of less than 8 F^2 size. This cell can support single bit access for read, write, and release modes.

[0057] Table 1 provides a summary of the operating modes and voltage conditions for a preferred NT-FET device for assumed relative capacitance values. Changing assumed capacitance ratios and applied voltages changes the select and release conditions of the NT-FET device. These values are CG to FGNT capacitance C_{12} equals C_{23}, the FGNT to FET channel capacitance. Depletion layer capacitance C_{36} equals 0.2 C_{23}. The much smaller release gate RG to FGNT capacitance C_{27} is less than 0.1 $C_{12,}$ and $C_{23,}$ and has minimal impact on the internal NT-FET voltage levels resulting from capacitance coupling. These capacitances are illustrated in Figure 3.

MODE/ CONDITION	V_{CG}	Vd	Vs	V_{FGNT*}	$V_{NT\ SELECT+}$	V_{RG}	$V_{NT\ RELEASE++}$
READ							
ON	1.0	1.0 float	0	1.0	0	0	- 1.0
OFF	1.0	1.0 float	0	0.5	0.5	0	- 0.5
WRITE "1"							
OFF -> ON	2.5	0	float	1.25	1.25	0	-1.25
WRITE "0"							
OFF -> OFF	2.5	1 – 2.5	float	2.1	0.4	0	-2.1
RELEASE							
BLOCK REL ON/OFF	0	any	any	0	0	6.5	$\|2.1\| < \& < 6.5$
BIT/NIBBLE REL RELEASE ON/OFF	0	any	any	0	0	6.5	$\|2.1\| < \& < 6.5$
NO RELEASE ON	3.5	1 – 2.5	float	3.5	0	6.5	$3 < \& < 6.5$
OFF	3.5	1 – 2.5	float	3.0	0.5	6.5	$3 < \& < 6.5$

* FET $V_{TH} = 0.7$ volts

Vd droops if NT-FET device is ON;
Vd unchanged if NT-FET device is OFF

\+ $V_{NT\ SELECT} = V_{CG} - V_{FGNT}$ Requirement $0.5 < V_{NT\ SEL\ TH} < 1.25$ volts

++ $V_{NT\ RELEASE} = V_{RG} - V_{FGNT}$ Requirements
Block Release: $|2.1| < V_{NT\ REL\ TH} < 6.5$** volts
Bit/Nibble Release: $3.5 < V_{NT\ REL\ TH} < 6.5$ volts

** Note: limited by RL driver; can go to 10 volts

[0058] The nanotube element of preferred devices may be constructed as explained in the following U.S. Patents and/or applications, all of which are incorporated by reference in their entirety. Preferred nanotube elements are made from a porous fabric of nanotubes. In certain embodiments, the fabric is highly porous and is substantially a monolayer of single-walled carbon nanotubes. See, e.g., U.S. Patent Nos. 6574130, 6643165, and 6706402; See also U.S. Patent Publication Nos. 2003-0021966, 2003-

0124325, 2003-0124837, and 2003-199172; and U.S. Patent Application Nos. 10/341005, 10/341054, 10/341055, 10/341130, 10/776059, and 10/776572.

[0059] In at least some cases, to create a nanofabric, the technique chosen must result in a sufficient quantity of nanotubes in contact with other nanotubes which thereby matte as a result of the nanotubes' adhesion characteristics. Certain embodiments (e.g., memory cells) benefit when the nanofabric is very thin (e.g., less than 2nm); for example, when the nanofabric is primarily a monolayer of nanotubes with sporadic overlapping (sometimes fabric will have portions that are bilayers or trilayers), or a multilayer fabric with relatively small diameter nanotubes. Moreover, many of these embodiments benefit when the nanotubes are single-walled nanotubes (SWNTs). Other embodiments (e.g., conductive traces) may benefit from thicker fabrics or multi-walled nanotubes (MWNTs). The nanofabric is patterned using photolithographic techniques generating an electrically conductive trace of nanotubes, NT.

[0060] Other embodiments may employ double-walled nanotubes, including such nanotubes with metallic properties.

[0061] The preferred embodiment uses electrostatic attractive forces to deflect the nanotube element, but other embodiments may use repulsive forces.

[0062] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of the equivalency of the claims are therefore intended to be embraced therein.

[0063] What is claimed is: